

**AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the subject application:

**Listing of Claims**

- 1 1. (Original) A method comprising:
  - 2 in response to a data read request for requested data:
    - 3 allocating an area of memory to the requested data, the memory
    - 4 area being divided into at least one memory chunk;
    - 5 writing a seed value to one or more of the at least one memory
    - 6 chunk; and
    - 7 in response to completion of at least one write transaction
    - 8 corresponding to the data read request, for each of the one
    - 9 or more memory chunks having a seed value, validating the
    - 10 integrity of each of the at least one write transaction based,
    - 11 at least in part, on the seed value.
  - 1 2. (Currently Amended) The method of claim 1, wherein said validating the
  - 2 integrity of a given one of the at least one write transaction comprises, for
  - 3 a given memory chunk:
    - 4 determining if the memory chunk includes the seed value; and

5 if the memory chunk includes the seed value, determining that a  
6 transmission error occurred ~~the given write transaction is invalid.~~

1 3. (Original) The method of claim 2, wherein said determining if the memory  
2 chunk includes the seed value comprises determining if the memory  
3 chunk includes the seed value at specified bits of the memory chunk.

1 4. (Currently Amended) The method of claim 2, additionally comprising  
2 modifying the seed value if it is determined that a transmission error  
3 occurred ~~the write transaction is determined to be invalid.~~

1 5. (Original) The method of claim 1, wherein the size of the seed value is  
2 based on a specified error rate of the device.

1 6. (Original) An apparatus comprising:  
2 circuitry capable of responding to a data read request for requested data  
3 by:

4 allocating an area of memory to the requested data, the memory  
5 area being divided into at least one memory chunk;

6 writing a seed value to one or more of the at least one memory  
7 chunk; and

8 responding to completion of at least one write transaction  
9 corresponding to the data read request by, for each of the  
10 one or more memory chunks having a seed value, validating  
11 the integrity of each of the at least one write transaction

12 based, at least in part, on the seed value.

1 7. (Currently Amended) The apparatus of claim 6, wherein said circuitry  
2 capable of validating the integrity of a given one of the at least one write  
3 transaction is capable of, for a given memory chunk:

4 determining if the memory chunk includes the seed value; and

5 if the memory chunk includes the seed value, determining that a

6 transmission error occurred ~~the given write transaction is invalid.~~

1 8. (Original) The apparatus of claim 7, wherein said circuitry capable of  
2 determining if the memory chunk includes the seed value is capable of  
3 determining if the memory chunk includes the seed value at specified bits  
4 of the memory chunk.

1 9. (Currently Amended) The apparatus of claim 7, wherein said circuitry is  
2 additionally capable of modifying the seed value if it is determined that a  
3 transmission error occurred ~~the write transaction is determined to be~~  
4 ~~invalid.~~

1 10. (Original) The apparatus of claim 6, wherein the size of the seed value is  
2 based on a specified error rate of the device.

1 11. (Currently Amended) A system comprising:

2 a PCI-E ~~(Peripheral Component Interconnect - Enhanced)~~ (Peripheral  
3 Component Interconnect - Express) bus;

4 a buffer communicatively coupled to the PCI-E bus, the buffer being  
5 divided into at least one memory chunk; and  
6 circuitry capable of responding to a data read request for requested data  
7 by:  
8 allocating the buffer to the requested data, the buffer being divided  
9 into at least one memory chunk;  
10 writing a seed value to one or more of the at least one memory  
11 chunk; and  
12 responding to completion of at least one write transaction  
13 corresponding to the data read request by, for each of the  
14 one or more memory chunks having a seed value, validating  
15 the integrity of each of the at least one write transaction  
16 based, at least in part, on the seed value.

1 12. (Currently Amended) The system of claim 11, wherein said circuitry  
2 capable of validating the integrity of a given one of the at least one write  
3 transaction is capable of, for a given memory chunk:  
4 determining if the memory chunk includes the seed value; and  
5 if the memory chunk includes the seed value, determining that a  
6 transmission error occurred ~~the given write transaction is invalid.~~

1 13. (Original) The system of claim 12, wherein said circuitry capable of  
2 determining if the memory chunk includes the seed value is capable of  
3 determining if the memory chunk includes the seed value at specified bits  
4 of the memory chunk.

1 14. (Currently Amended) The system of claim 12, wherein said circuitry is  
2 additionally capable of modifying the seed value if it is determined that a  
3 transmission error occurred ~~the write transaction is determined to be~~  
4 ~~invalid.~~

1 15. (Original) The system of claim 11, wherein the size of the seed value is  
2 based on a specified error rate of the device.

1 16. (Original) An article comprising a machine-readable medium having  
2 machine-accessible instructions, the instructions when executed by a  
3 machine, result in the following:

4 responding to a data read request for requested data by:

5 allocating an area of memory to the requested data, the memory  
6 area being divided into at least one memory chunk;

7 writing a seed value to one or more of the at least one memory  
8 chunk; and

9 responding to completion of at least one write transaction

10 corresponding to the data read request by, for each of the

11 one or more memory chunks having a seed value, validating

12 the integrity of each of the at least one write transaction  
13 based, at least in part, on the seed value.

1 17. (Currently Amended) The article of claim 16, wherein said instructions that  
2 result in validating the integrity of a given one of the at least one write  
3 transaction comprise instructions that result in, for a given memory chunk:  
4 determining if the memory chunk includes the seed value; and  
5 if the memory chunk includes the seed value, determining that a  
6 transmission error occurred ~~the given write transaction is invalid.~~

1 18. (Original) The article of claim 17, wherein the instructions that result in  
2 determining if the memory chunk includes the seed value comprise  
3 instructions that result in determining if the memory chunk includes the  
4 seed value at specified bits of the memory chunk.

1 19. (Currently Amended) The article of claim 17, additionally comprising  
2 instructions that result in modifying the seed value if it is determined that a  
3 transmission error occurred ~~the write transaction is determined to be~~  
4 ~~invalid.~~

1 20. (Original) The article of claim 16, wherein the size of the seed value is  
2 based on a specified error rate of the device.